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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/015,972	11/01/2001	Steven D. Roach	LT-146	6870

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EXAMINER	
TSAI, CAROL S W	
ART UNIT	**PAPER NUMBER**
2857	

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/015,972	ROACH, STEVEN D.	
	Examiner	Art Unit	
	Carol S Tsai	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,17-25 and 36-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-25 and 37-42* is/are allowed.

6)☒ Claim(s) *1-3 and 36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 27, 2004 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3 and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by U. S. Patent No.4,222,127 to Fukaya et al.

With respect to claims 1-3, and 36, Fukaya et al. disclose a method for determining a current supplied by an integrated circuit comprising: determining a first voltage drop across a termination impedance with respect to a reference voltage (see Fig. 4 and col. 5, lines 53-64); comparing a second voltage drop across a first impedance on the integrated circuit with a third voltage drop across a second impedance on the integrated circuit, wherein the first impedance is different from the second impedance

(see Fig. 4 and col. 5, line 64 to col. 6, line 11); and processing information obtained in the determining and comparing steps, wherein the information is based on the first, second, and third voltages, to obtain a value for the supplied current (see Fig. 4 and col. 4, lines 16-64 and col. 6, lines 11-56).

Allowable Subject Matter

4. Claims 17-25 and 37-42 allowed.

5. U. S. Patent No. 4,222,127 to Fukaya et al. is the reference closest to the claimed invention. Fukaya et al. disclose a circuit for determining a current supplied by an integrated circuit comprising: determining a first voltage drop across a termination impedance with respect to a reference voltage; comparing a second voltage drop across a first impedance on the integrated circuit with a third voltage drop across a second impedance on the integrated circuit, wherein the first impedance is different from the second impedance; and processing information obtained in the determining and comparing steps, wherein the information is based on the first, second, and third voltages, to obtain a value for the supplied current. However, Fukaya et al. do not teach a sensing impedance disposed on the integrated circuit; and a modulation impedance; a first measurement device coupled to the modulation and sensing impedances and configured to measure a first voltage drop across a termination impedance; a termination impedance a second measurement device coupled to the termination impedance and configured to measure a second voltage drop across the termination impedance; and processing circuitry configured to receive the first and second voltage drops measured by the first

and second measurement devices, respectively, and to calculate supplied current therefrom; and including all of the other limitations in the respective independent claims.

6. U. S. Patent No. 4,222,127 to Fukaya et al. is the reference closest to the claimed invention. Fukaya et al. disclose a method for determining a current supplied by an integrated circuit comprising: determining a first voltage drop across a termination impedance with respect to a reference voltage; comparing a second voltage drop across a first impedance on the integrated circuit with a third voltage drop across a second impedance on the integrated circuit, wherein the first impedance is different from the second impedance; and processing information obtained in the determining and comparing steps, wherein the information is based on the first, second, and third voltages, to obtain a value for the supplied current. However, Fukaya et al. do not teach calculating a first value by dividing the value of the second impedance by the value of the first impedance, calculating a second value by dividing the value of the voltage drop across the termination impedance by the value of the reference voltage, calculating a third value by dividing the value of the reference voltage by the value of the termination impedance, calculating a fourth value by dividing the value of the voltage drop across the first impedance by the value of the reference voltage, calculating a fifth value by dividing the value of the voltage drop across the second impedance by the value of the reference voltage, and wherein the comparing further comprises calculating a sixth value by dividing the voltage drop across the first impedance by the voltage drop across the second impedance; and including all of the other limitations in the respective independent claims.

7. U. S. Patent No. 4,222,127 to Fukaya et al. is the reference closest to the claimed invention. Fukaya et al. disclose a method for determining a current supplied by an integrated circuit comprising: determining a first voltage drop across a termination impedance with respect to a reference voltage; comparing a second voltage drop across a first impedance on the integrated circuit with a third voltage drop across a second impedance on the integrated circuit, wherein the first impedance is different from the second impedance; and processing information obtained in the determining and comparing steps, wherein the information is based on the first, second, and third voltages, to obtain a value for the supplied current. However, Fukaya et al. do not teach an off-chip impedance, not disposed on the integrated circuit, having a known resistance; a source impedance disposed on the integrated circuit, wherein a first terminal of the source impedance is coupled to a first terminal of the off-chip impedance; a modulation impedance disposed on the integrated circuit, wherein a second terminal of the modulation impedance is coupled to a second terminal of the off-chip impedance; a first measurement device for measuring an off-chip voltage drop across the off-chip impedance with respect to a reference voltage; a second measurement device a source voltage drop across the source impedance with respect to a modulation voltage drop across the modulation impedance; and processing circuitry configured to determine the bias current based on the measurements of for measuring the first and Second measurement devices; and including all of the other limitations in the respective independent claims.

8. U. S. Patent No. 4,222,127 to Fukaya et al. is the reference closest to the claimed invention. Fukaya et al. disclose a method for determining a current supplied by an

integrated circuit comprising: determining a first voltage drop across a termination impedance with respect to a reference voltage; comparing a second voltage drop across a first impedance on the integrated circuit with a third voltage drop across a second impedance on the integrated circuit, wherein the first impedance is different from the second impedance; and processing information obtained in the determining and comparing steps, wherein the information is based on the first, second, and third voltages, to obtain a value for the supplied current. However, Fukaya et al. do not teach a method for controlling the amount of output power provided by an integrated circuit, the method comprising: measuring a first voltage drop across an off-chip impedance with respect to a reference voltage, wherein the off-chip impedance is not disposed on the integrated circuit, and the off-chip impedance has a known resistance; measuring a second voltage drop across a source impedance with respect to a third voltage drop across a modulation impedance, wherein the source and modulation impedances are disposed on the integrated circuit; determining a bias current based on the first, second and third voltage measurements; and adjusting the bias current based on the determined bias current to control the amount of output power provided by the integrated circuit.

Response to Arguments

9. Applicant's arguments with respect to claims 1-3 and 36 have been considered but are moot in view of the new ground(s) of rejection.

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carol S. W. Tsai whose telephone number is (571) 272-2224. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571) 272-2216. The fax number for TC 2800 is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2800 receptionist whose telephone number is (571) 272-1585 or (571) 272-2800.

In order to reduce pendency and avoid potential delays, Group 2800 is encouraging FAXing of responses to Office actions directly into the Group at (703) 872-9306. This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2800 will be promptly forwarded to the examiner.

Carol S. W. Tsai
Patent Examiner
Art Unit 2857

10/15/04